Notice of Allowability	Application No.	Applicant(s)	
	10/797,537	NAIR ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the appeal brief filed 5/23/06*.

2. ☒ The allowed claim(s) is/are *1-4,6 and 8-21*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Kevin Jackson on August 17, 2006.

The application has been amended as follows:

Claims:

1. A lateral IGFET device comprising: semiconductor substrate having a first conductivity type; a region of semiconductor material comprising alternating layers of first and second conductivity type material deposited over the semiconductor substrate and having a first major surface, the region of semiconductor material further including a top layer of the first conductivity type formed adjacent the first major surface and one of the alternating layers of the second conductivity type formed adjacent and below the top layer; a drain region of the second conductivity type extending from the first major surface into at least a portion of the region of semiconductor material and adjoining at least a portion of the alternating layers; a body region of the first conductivity type formed in a portion of the region of semiconductor material and extending from the first major surface partially into the top layer; a first source region formed in the body region; ~~and~~ a trench gate structure formed in a portion of the region of semiconductor material

and adjoining the alternating layers, the body region and the first source region, wherein the trench gate structure controls a sub-surface channel region; and a surface gate structure including a gate dielectric layer formed overlying t-he first major surface and a gate electrode layer over-lying the gate dielectric layer, wherein the surface gate structure extends over the first source region and controls conduction in a surface channel region.

Claim 5 is cancelled.

10. A lateral MOSFET device comprising: a semiconductor substrate; a region of semiconductor material including a plurality of alternating layers of first and second conductivity semiconductor material formed ~~over~~ overlying the semiconductor substrate and having a major surface; a trench drain structure formed in the region of semiconductor material; a body region of the first conductivity type formed in the region of semiconductor material; a source region of the second conductivity type formed in the body region; a trench gate structure formed in the region of semiconductor material adjoining at least a portion of the alternating layers, the body region and the source region, wherein the trench gate structure controls a sub-surface channel region; and a surface gate structure including a gate dielectric layer and a gate conductive portion formed overlying the major surface and adjacent the body region and the source region, wherein the surface gate structure controls a surface channel region. ~~; a body region of first conductivity type formed adjacent the trench gate structure and the surface gate~~

~~structure, and a source region of the second conductivity type formed in the body region.~~

Allowable Subject Matter

Claims 1-4,6 and 8-21 are allowed.

The following is an examiner's statement of reasons for allowance: Claims 1-4,6 and 8-16 are allowable because prior art does not show alone or in combination along with the limitations of the independent claims such as a drain region of the second conductivity type extending from the first major surface into at least a portion of the region of semiconductor material and adjoining at least a portion of the alternating layers; a body region of the first conductivity type formed in a portion of the region of semiconductor material and extending from the first major surface partially into the top layer and a trench gate structure formed in a portion of the region of semiconductor material and adjoining the alternating layers, the body region and the first source region, wherein the trench gate structure controls a sub-surface channel region; and a surface gate structure including a gate dielectric layer formed overlying t-he first major surface and a gate electrode layer over-lying the gate dielectric layer, wherein the surface gate structure extends over the first source region and controls conduction in a surface channel region.

Claims 17-21 are allowable because prior art does not disclose alone or in combination along with the limitations of the independent claim such as a doped region

of the second conductivity type formed along a sidewall of the trench gate structure and extending into the semiconductor region below the body region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KLR

Zandra V. Smith
Supervisory Patent Examiner
16 Aug - 2006